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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,748	02/22/2002	Harlan T. Beverly	ITL.0703US (P13939)	9386

21906 7590 05/21/2007

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EXAMINER	
MERED, HABTE	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
05/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/081,748	BEVERLY ET AL.	
	Examiner	Art Unit	
	Habte Mered	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 02/22/2007 has been entered and fully considered.

2. Claims 1-22 remain pending. Claims 23-55 are cancelled. The base independent claims are 1 and 11.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 2, 10-13, 15, 17, and 19-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Kincaid (US 6, 640, 275).

Kincaid teaches system and method for data transfer between buses having different speeds.

3. Regarding **claims 1 and 11**, Kincaid teaches a method and device comprising: receiving a data frame of a first size **(See Figure 5, from ingress data 500 frames of 32 bits enter demux 505)**; demultiplexing the data frame **(See Figure 5, element 505)**; writing blocks of the demultiplexed data frame at the first size into a register **(Figure 5, blocks of 32 bits are written in data transfer registers 510)**; reading blocks of a second size, different from the first size, from the register **(Figure 5, Blocks of 64 bits**

are read from data registers 510); and multiplexing the blocks **(Figure 5, element 511)** to form an output data frame of the second size. **(Blocks of 64 bits are formed as an output of Figure 5, element 511 – See also Column 5:5-55)**

4. Regarding **claims 2, 10, and 15**, Kincaid teaches a method and device wherein receiving a data frame of a first size includes receiving a 64-bit data frame at the demultiplexer and the multiplexer outputs a data frame of 66-bits. **(Kincaid discloses in Column 2:46-50 that the received input signal can be any size. He indicates converting a block of 32 bits to a block of 64 bits is an example and his method is applicable to converting block size to accommodate data transfer between two buses having two different speeds including 64-bits and 66-bits data buses.)**

5. Regarding **claim 17**, Kincaid teaches a device using a multiplexer as shown in Figure 5. **(In the discussions in Column 2:46-50 it is clear that Kincaid's system can accommodate different frame formats and to accomplish such a task it is inherent to use various types of multiplexers including 32:1 muxs. Examiner takes Official Notice in indicating that use of a thirty-two to one multiplexer is well known as indicated for instance in Tomar et al (US 6, 944, 190) in Figure 10 and Column 13:50-67.)**

6. Regarding **claim 12**, Kincaid discloses a device that includes a first counter **(Figure 5, element 506)** to control the writing of data from the demultiplexer to the register.

7. Regarding **claim 13**, Kincaid discloses a device that includes a second counter **(Figure 5, element 508)** to control the reading of data from the register to the multiplexer.

8. Regarding **claim 19**, Kincaid discloses a device wherein the multiplexer reads data from the register in 66-bit blocks. **(This can easily be accommodated by Kincaid 's system when implementing it as a system for transferring data between a 64-bits wide data bus and a 66-bits wide data bus)**

9. Regarding **claim 20**, Kincaid discloses a device wherein the demultiplexer **(See Figure 5, element 505)** writes data in blocks of a first size **(See Figure 5, block size of 32 bits)** to the register **(See Figure 5, element 510)** and the multiplexer **(Figure 5, element 511)** reads data in blocks of a second size **(Figure 5, Block size of 64 bits)**, different from the first size from the register.

10. **Claims 1, 11, 21, and 22** are rejected under 35 U.S.C. 102(e) as being anticipated by Walker et al (US Pub. No. 2004/0228364), hereinafter referred to as Walker.

Walker like Kincaid teaches system and method for data transfer between buses having different speeds.

11. Regarding **claims 1 and 11**, Walker discloses a method and device comprising: receiving a data frame of a first size **(Figure 8B, element 310 receiving a data frame of size 32 bits (i.e. quad) and last line in Paragraph 133)**; demultiplexing the data frame **(Figure 8B, elements 303, 311, 312 – demultiplexed into blocks 32 bits)**; writing blocks of the demultiplexed data frame at the first size into a register **(Figure 8B,**

elements 311, 312 and 304); reading blocks of a second size **(Figure 8B, elements 313 and 304 – blocks of 64 bits)**, different from the first size **(Figure 8B, element 311, 32 bits)**, from the register **(Figure 8B, element 304)**; and multiplexing the blocks to form an output data frame of the second size **(Figure 8B, element 308 is the assembler and is shown to contain a multiplexer in Figure 1, element 34 as discussed in Paragraphs 142.) (See also Paragraphs 133 to 142 for a detailed discussion.) (Examiner wants to point out that the Applicant in the Remarks, page 10, and paragraph 5 of the amendment filed on 2/8/2006 indicated that in Walker's system there is nothing that indicated the size of the blocks written into register 304 is different from the size of the blocks read from register 304. Walker clearly indicates in paragraphs 41 and 134 the input to the register 304 is a quad (i.e. block of eight words or 32 bits) and in paragraph 135, lines 4-6, clearly shows what is read out of the register is formed from a pair of quads (i.e. a block of 64-bits)**

12. Regarding **claim 21**, Walker discloses a device wherein the device is part of a physical coding sub layer. **(See Paragraph 33 and Figure 1, element 14)**

13. Regarding **claim 22,** Walker discloses a device wherein the device is part of a receiver in a fiber optic network. **(See Paragraph 49)**

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 3 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Chen (US 4, 121, 217).

Kincaid teaches all aspects of the claimed invention as set forth in the rejections of claims 2 and 11 respectively but fails to expressly teach the use of a one to thirty-three demultiplexer.

Chen teaches various interface units for data transmission networks.

Chen teaches the use of one to thirty-three demultiplexer. **(See Figure 13, element 252)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kincaid's apparatus to incorporate the use of one to thirty-three demultiplexer, the motivation being it would allow his system to combine and separate telecom pipes that carry 32 channels such as E1 pipes with ease and added flexibility.

3. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Chen as applied to claim 3 above, and further in view of Ryan (US 6, 560, 669).

33. Regarding **claim 4**, the combination of Kincaid and Chen teaches all aspects of the claimed invention as set forth in the rejections of claim 3 but fails to teach expressly writing blocks of 64 bits into memory.

Ryan teaches a method and apparatus for performing a block write to a memory device.

Ryan discloses writing blocks of 64 bits into memory. **(See Figure 10, elements 130 and 124 and also Column 7, Lines 5-20)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Kincaid's and Chen's apparatus to incorporate writing blocks of 64 bits into memory, the motivation being in the telecom world a frame of size 64 bits is common for ISDN BRI and PRI systems as well as systems based on DSLs and Kincaid's system would be required to support these applications as his system supports any protocol.

4. Regarding **claim 5**, Kincaid discloses a method wherein writing the blocks into a register include writing 2,112 bits into a register. **(Determining memory size is a design choice. The Court has rendered a decision indicating that change in size is a design decision In re Rose, 105 USPQ 237 (CCPA 1955) and specifically states the following in the decision: "...We do not feel that this limitation is patentably significant since at most relates to the size of the article under consideration which is not ordinarily a matter of invention.")**

5. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Ryan (US 6, 560, 669).

Kincaid teaches all aspects of the claimed invention as set forth in the rejections of claim 11 but fails to teach writing blocks of 64 bits into memory.

Ryan discloses writing blocks of 64 bits into memory. **(See Figure 10, elements 130 and 124 and also Column 7, Lines 5-20)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kincaid's apparatus to incorporate writing blocks of 64 bits into memory, the motivation being in the telecom world a frame of size 64 bits is common for ISDN BRI and PRI systems as well as systems based on DSLs and Kincaid's system would be required to support these applications as his system supports any protocol.

6. **Claims 6-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Chen and Ryan as applied to claim 5 above, and further in view of Agere (Agere Systems, "10 Gigabit Ethernet PCS Intellectual Property Cores", Preliminary Data Sheet, July 2001).

7. Regarding **claim 6**, the combination of Kincaid, Chen, and Ryan teaches all aspects of the claimed invention as set forth in the rejections of claim 5 but fails to teach controlling a write pointer at a frequency of approximately 161 MegaHertz.

Agere provides data sheet for a product called ORLI10G.

Agere discloses a method including controlling a write pointer at a frequency of approximately 161 MegaHertz. **(See Figure 1, RxPLL writing at 161 MHz)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Kincaid's, Chen's and Ryan's apparatus to incorporate a method including controlling a write pointer at a frequency of approximately 161 MHz, the motivation being using a write pointer at such a rate allows the system to write data in the buffer at a slower rate than the incoming rate and consequently helps in minimizing data loss.

8. Regarding **claim 7**, Kincaid discloses a method wherein reading blocks of the second size includes reading blocks of sixty-six bits from the register. **(This is a consequence of trying to convert t format acceptable by a 66-bits wide bus of which Kincaid is capable of handling as stated in Column 2:46-51)**

9. Regarding **claim 8**, Kincaid discloses a method including controlling a read pointer at a frequency of approximately 156 MegaHertz. **(This is strictly a design issue but is already disclosed by Agere in Figure 1 reading at 156.25 MHz and on page 3 in the section describing the gearbox.)**

10. Regarding **claim 9**, Kincaid discloses a method of wherein multiplexing the blocks to form an output data frame of a second size includes forming an output data frame by using a thirty-two to one multiplexer. **(Determining multiplexer size is a design choice. The Court has rendered a decision indicating that change in size is a design decision In re Rose, 105 USPQ 237 (CCPA 1955) and specifically states the following in the decision: "...We do not feel that this limitation is patentably significant since at most relates to the size of the article under consideration which is not ordinarily a matter of invention." Examiner also takes Official Notice in indicating that use of a thirty-two to one multiplexer is well known as indicated for instance in Tomar et al (US 6, 944, 190) in Figure 10 and Column 13, Lines 50-67.)**

11. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid in view of Agere (Agere Systems, "10 Gigabit Ethernet PCS Intellectual Property Cores", Preliminary Data Sheet, July 2001).

Kincaid fails to teach controlling a write pointer at a frequency of approximately 161 MHz and reading at 156 MHz.

Agere discloses a method including controlling a write pointer at a frequency of approximately 161 MHz and reading at 156 MHz. **(See Figure 1, RxPLL2 writing at 161 MHz and Gearbox reading at 156.25 Mhz from RxPLL and on page 3 in the section describing the gearbox.)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kincaid's apparatus to incorporate a method including controlling a write pointer at a frequency of approximately 161 MHz and reading at approximately 156 MHz, the motivation being using a write pointer at such a rate allows the system to write data in the buffer at a slower rate than the incoming rate and consequently helps in minimizing data loss.

Response to Arguments

1. Applicant's arguments filed on 2/22/2007 have been fully considered but they are not persuasive.

2. In the Remarks, on page 5 in the 2nd paragraph, with respect to Independent claim 1, Applicant argues that Kincaid fails to disclose a demultiplexer and fails to teach what is called for in claim 1 namely demultiplexing of the received data frame. Further, Applicant indicates element 505 is a multiplexer and cites column 5, line 13.

Examiner respectfully disagrees with Applicant's conclusions. It is the position of the Examiner that Kincaid teaches what is claimed in claim 1 namely the demultiplexing of the received signal and shows element 505 is a demultiplexer in Figure 5. First, the

symbol associated with element 505 is well known in the art and is only used to represent a demultiplexer. Second, a close review of Figure 5 shows the functionality of element 505 is strictly demultiplexing the input frame 500 into at least four components and again without doubt element 505 is a demultiplexer. Third, even though Kincaid in Column 5, line 13 refers to element 505 in Figure 5 as a multiplexer, he clearly indicates that in subsequent lines, i.e. Column 5, Lines 13-25 the so called multiplexer routes or demultiplexes the received ingress frame 500 to various registers 510 in Figure 5 again functioning as a demultiplexer. Further a close review of Kincaid's diagrams (i.e. Figures 1 and 2) and text clearly shows that whom ever wrote the Kincaid's Patent Application consistently refers as multiplexer to elements providing demultiplexing functionality and vice versa. The labels multiplexers and demultiplexers are irrelevant as long as one can clearly show the element in question (i.e. Figure 5, 505) has the demultiplexing functionality and Kincaid in fact just teaches precisely that is the case. Therefore, given these strong points against Applicant's arguments, Examiner is maintaining the 102 rejections of claims 1 and 11 based on Kincaid's teachings.

3. In the Remarks, on page 5, in the last paragraph, with respect to independent claim 11, Applicant argues that Kincaid fails to teach the limitation that calls for a multiplexer that changes the size of a data frame. Further, Applicant argues Kincaid teaches only a structure that puts together quads to form a data frame, which is then not size converted.

Examiner respectfully disagrees with Applicant's conclusions. First, Kincaid in fact teaches an element in Figure 5 that has multiplexing functionality and changes the

size of a data frame to 64 bits different from the received 32-bit frame. The element that has the multiplexing functionality is element 511 in Figure 5 and element 511 is represented as a multiplexer in Figure 5. Further Applicant's argument based on Kincaid teaching putting together quads is incorrect, as it does not do that and Applicant has not cited support in Kincaid teaching Applicant's position. Hence again, Examiner is maintaining the 102 rejection of claim 11 based on Kincaid's teachings.

4. In the Remarks, on page 5, in paragraphs 4 and 5, with respect to independent claim 1, Applicant argues first that Examiner is re-introducing a reference, i.e. Walker that was withdrawn previously. Applicant argues, in the Remarks in paragraph 4, Walker fails to teach the required limitation in claim 1 that calls for receiving a data frame of first size. Applicant further argues in Paragraph 5 that all Walker is teaching is formation of a frame. Applicant further goes on to say element 100 (i.e. without indicating which figure contains element 100) is simply a continuous stream of quads and cites paragraph 43 as giving support to Applicant's position. The Applicant restates that there is no changing of frame size but merely the assembling of a frame.

Examiner respectfully disagrees with Applicant's conclusion. It is correct Walker was re-introduced as a reference after it was initially withdrawn from a previous Office Action. To set the record clear, Examiner when re-introducing Walker in the last Office Action provided how the Examiner upon further review determined how Walker adequately addressed the arguments raised by the Applicant against using Walker in the Remarks dated 2/08/2006. In the Remarks dated 2/08/2006 Applicant's central argument stated in paragraph 5 of page 10 and in paragraph 4 of page 11 is that the

block size is never changed contrary to the claim limitation calling for the frame size to be changed. In the last Office Action in item 15, Examiner addressed how the block size is changed. Nevertheless, the Applicant has reformulated the same arguments in the current Remark dated 2/22/2007. Below, Examiner will again address all issues raised by the Applicant over Walker as a prior art in the subsequent paragraphs.

Applicant suggests that Walker's embodiment shown in Figure 8B does not receive a data frame of first size. In fact Applicant indicates let alone receiving a frame it is not at all formed until it reaches element 308. Applicant agrees as stated in the Remarks in the 5th paragraph of page 10 that in Figure 8B a continuous stream of quads is received and is shown as element 36 in Figure 8B. There is no dispute that the quads are 32 bits (This is further supported by the last four lines of paragraph 41 and in fact Applicant has agreed to the same definition as stated in the previous Remarks dated 2/08/2006 in paragraph 6 of page 10). The Applicant is simply arguing that the quad is not a frame. A frame is defined in the art as a packet that has delimiters that indicate the start and end of a packet. Any data communication book readily supports this definition and Examiner cites Newton's Telecom Dictionary (16th edition see pages 357-358). Clearly Walker shows his quads have a start packet (S) and end packet (T) as clearly indicated in paragraph 40, Figures 2 and 3D and are as some examples indicating Walker's quads can really be considered as a frame.

Given that Walker's Figure 8B receives a frame of 32 bits (i.e. quad of 32 bits) the next issue is to see if the received frame is demultiplexed as called for in claim 1. Indeed Walker in Figure 8B shows that received frame of 32 bits is demultiplexed by

element 303. As claim 1 requires the demultiplexed data is written as a first size (i.e. 32 bits) into register 304 and a block of 64 bits is read from the register as clearly shown in Figure 8B. Walker further supports this in paragraphs 41 and 134 indicating the input to the register 304 is a quad (a block of 8 words or 32 bits) and in paragraph 135, lines 4-6, Walker clearly shows what is read out of the register is formed from a pair of quads (i.e. block of 64 bits). From the perspective of Figure 1, element 100 is actually Figure 8B and as is called for in claim 1 the final output is fed to a multiplexer 34 of Figure 1 which Applicant readily agrees that is the case in the Remarks in paragraph 5 of page 5.

Hence Examiner has clearly shown how a data frame of 32 bits is received and finally converted into a frame of 66 bits using the teachings of Walker. Hence, the Examiner believes all issues raised by the Applicant has been addressed and the prior art. i.e. Walker, adequately teaches all the limitations of claims 1 and 11. Therefore the 102 rejections of claims 1 and 11 based on Walker's teachings is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following adequately anticipate claims 23 and 33 that deal with means to detect synchronization bits using shift registers and logic gates:

US Patent (6, 275, 552) to Ando

US Patent (4, 748, 623) to Fujimoto

US Patent (5, 018, 140) to Lee et al

US Patent (4, 404, 675) to Karchevski

US Patent (6, 163, 423) to Lee et al

US Pub. No. (2002/0110208 A1) to Suzuki

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H. To can be reached on 571 272 7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Habte Mered
5-9-2007

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